WHAT IS CLAIMED IS:

1. A power monitor circuit capable of notifying processing circuits operating from a first power supply having a VDD output voltage when a second power supply having a VDDIO output voltage is powered up, wherein VDDIO is greater than VDD, said power monitor circuit comprising:

a voltage divider circuit coupled between said second power supply and ground and having an output node that rises to a high voltage when said second power supply is powered up; and

an odd number of serially connected inverters operating from said first power supply, wherein an input of a first of said serially connected inverters is connected to said voltage divider circuit output node and an output of a last of said serially connected inverters produces a status signal that is low when said voltage divider circuit output node is high and is high when said voltage divider circuit output node is low, and wherein said status signal is an input signal to said voltage divider circuit operable to minimize DC current consumption in said voltage divider circuit when said second power supply is powered up while maintaining a value of said status signal.

2. The power monitor circuit as set forth in Claim 1 wherein said serially connected inverters comprise CMOS inverters.

3. The power monitor circuit as set forth in Claim 1 wherein said voltage divider circuit comprises: 1) a first N-channel transistor having a gate and a drain coupled to said VDDIO output voltage and a source coupled to said voltage divider circuit output node; 2) a second N-channel transistor having a gate coupled to said VDD output voltage and a drain coupled to said voltage divider circuit output node; and 3) a third N-channel transistor having a gate coupled to said status signal, a drain coupled to a source of said second N-channel transistor, and a source coupled to ground.

4. The power monitor circuit as set forth in Claim 3 further comprising a capacitor coupled between said voltage divider circuit output node and ground.

5. The power monitor circuit as set forth in Claim 4 further comprising a fourth N-channel transistor having a gate coupled to said VDD output voltage, a drain coupled to said VDDIO output voltage, and a source coupled to said voltage divider circuit output node.

6. The power monitor circuit as set forth in Claim 1 wherein said odd number of serially connected inverters comprises one inverter.

7. The power monitor circuit as set forth in Claim 6 wherein said odd number of serially connected inverters comprises one CMOS inverter.

8. The power monitor circuit as set forth in Claim 1 wherein said odd number of serially connected inverters comprises three inverters.

9. The power monitor circuit as set forth in Claim 8 wherein said odd number of serially connected inverters comprises three CMOS inverters.

10. The power monitor circuit as set forth in Claim 1 wherein said odd number of serially connected inverters comprises five inverters.

11. The power monitor circuit as set forth in Claim 10 wherein said odd number of serially connected inverters comprises five CMOS inverters.

12. An integrated circuit comprising:

core processing circuitry operating from a first power supply having a VDD output voltage;

output stage circuitry operating from a second power supply having a VDDIO output voltage, wherein VDDIO is greater than VDD; and

a power monitor circuit capable of notifying said core processing circuitry when said second power supply having said VDDIO output voltage is powered up, said power monitor circuit comprising:

a voltage divider circuit coupled between said second power supply and ground and having an output node that rises to a high voltage when said second power supply is powered up; and

an odd number of serially connected inverters operating from said first power supply, wherein an input of a first of said serially connected inverters is connected to said voltage divider circuit output node and an output of a last of said serially connected inverters produces a status signal that is low when said voltage divider circuit output node is high and is high when said voltage divider circuit output node is low, and wherein said status signal is an input signal to said voltage divider circuit operable to minimize DC current consumption in said voltage divider

circuit when said second power supply is powered up while maintaining a value of said status signal.

13. The integrated circuit as set forth in Claim 12 wherein said serially connected inverters comprise CMOS inverters.

14. The integrated circuit as set forth in Claim 12 wherein said voltage divider circuit comprises: 1) a first N-channel transistor having a gate and a drain coupled to said VDDIO output voltage and a source coupled to said voltage divider circuit output node; 2) a second N-channel transistor having a gate coupled to said VDD output voltage and a drain coupled to said voltage divider circuit output node; and 3) a third N-channel transistor having a gate coupled to said status signal, a drain coupled to a source of said second N-channel transistor, and a source coupled to ground.

15. The integrated circuit as set forth in Claim 14 further comprising a capacitor coupled between said voltage divider circuit output node and ground.

16. The integrated circuit as set forth in Claim 15 further comprising a fourth N-channel transistor having a gate coupled to said VDD output voltage, a drain coupled to said VDDIO output voltage, and a source coupled to said voltage divider circuit output node.

17. The integrated circuit as set forth in Claim 12 wherein said odd number of serially connected inverters comprises one inverter.

18. The integrated circuit as set forth in Claim 17 wherein said odd number of serially connected inverters comprises one CMOS inverter.

19. The integrated circuit as set forth in Claim 12 wherein said odd number of serially connected inverters comprises three inverters.

20. The integrated circuit as set forth in Claim 19 wherein said odd number of serially connected inverters comprises three CMOS inverters.

21. The integrated circuit as set forth in Claim 20 wherein said odd number of serially connected inverters comprises five inverters.

22. The integrated circuit as set forth in Claim 21 wherein said odd number of serially connected inverters comprises five CMOS inverters.